**AMENDMENTS TO THE CLAIMS**

**(IN REVISED FORMAT COMPLIANT WITH THE PROPOSED REVISION TO 37 CFR 1.121)**

1. (CURRENTLY AMENDED) A system for designing an integrated circuit (IC) comprising:

a functional portion comprising an FPGA core;

a logic portion (i) connected to said functional portion and (ii) configured to (a) detect errors when in a first mode, (b) fix errors when in a second mode and ~~or~~ (c) verify fixes of errors in said functional portion when in a third mode, wherein said logic portion includes one or more interfaces;

a debugging/bug fix circuit configured to detect errors in said logic portion through said one or more interfaces; and

a diagnostic architecture using said FPGA core in a system on a chip design.

2. (CANCELED)

3. (CANCELED)

4. (PREVIOUSLY PRESENTED) The system according to claim 1, wherein said system is further configured to (i) provide ease in

bringing up, (ii) verification and (iii) debugging, each by interconnecting said circuit and said debugging/bug fix circuit.

5. (ORIGINAL) The system according to claim 1, wherein said system is further configured to provide one or more programming options of said circuit.

6. (PREVIOUSLY PRESENTED) The system according to claim 1, wherein said system is further configured to allow observation of one or more signals by said debugging/bug fix circuit.

7. (ORIGINAL) The system according to claim 6, wherein said system is further configured to allow observation of said one or more signals when running in a normal mode.

8. (ORIGINAL) The system according to claim 1, wherein said system is further configured to run in a single step mode.

9. (ORIGINAL) The system according to claim 8, wherein said system is further configured to run in said single step mode when controlled by a gate or a core.

10. (CANCELED)

11. (ORIGINAL) The system according to claim 9, wherein said core is programmable.

12. (PREVIOUSLY PRESENTED) The system according to claim 1, wherein said debugging/bug fix circuit comprises a debugging workstation.

13. (PREVIOUSLY PRESENTED) The system according to claim 1, wherein said debugging/bug fix circuit is further configured to allow one or more debugging features.

14. (ORIGINAL) The system according to claim 13, wherein said one or more debugging features support triggering and tracing based on one or more internal signals.

15. (ORIGINAL) The system according to claim 13, wherein said one or more debugging features support dynamically changing host register values.

16. (ORIGINAL) The system according to claim 13, wherein said one or more debugging features provide complex monitoring functions.

17. (ORIGINAL) The system according to claim 1, wherein said system is further configured to reduce debugging/verification time and/or improve product time to market.

18. (ORIGINAL) The system according to claim 1, wherein said circuit is further configured to operate in a normal mode and a single step mode.

19. (ORIGINAL) The system according to claim 18, wherein said normal mode is configured to allow said circuit to present one or more internal signals of said functional portion and said single step mode is configured to provide a plurality of signals of said functional portion.

20. (ORIGINAL) The system according to claim 18, wherein a scan chain is used to diagnose or fix a bug via the logic portion.

21. (PREVIOUSLY PRESENTED) The system according to claim 19, wherein the logic portion is further configured to bridge one or more of said plurality of signals between a plurality of modules.

22. (ORIGINAL) The system according to claim 1~~2~~, wherein said debugging/bug fix circuit and said circuit are configured to generate one or more debugging features.

23. (PREVIOUSLY PRESENTED) The system according to claim 1, wherein said debugging/bug fix circuit is configured to work with Computer Aided Design (CAD) software to provide one or more diagnostic functions.

24. (ORIGINAL) The system according to claim 23, wherein said diagnostic functions are selected from the group consisting of searching for a specific signal pattern~~, tracing the internal state machine~~, triggering on a programmed condition and other appropriate diagnostic functions.

25. (ORIGINAL) The system according to claim 23, wherein said diagnostic functions are selected from the group consisting of on the fly monitoring of a correctness of a bus protocol, and implementing statistics counting to measure ~~the~~ performance and ~~the~~ testing coverage.

26. (CURRENTLY AMENDED) A method for diagnostics comprising the steps of:

(A) interfacing a chip with an FPGA core;

(B) presenting one or more internal signals of said chip;

(C) verifying bugs when in a first mode and ~~or~~ fixing bugs when in a second mode in said chip with said one or more internal signals; and

(D) programming the FPGA core to dump data from a host register every N clock cycles.

27. (ORIGINAL) A computer readable medium configured to store instructions for executing the steps of claim 26.

28. (PREVIOUSLY PRESENTED) The method according to claim 26, further comprising:

capturing signals every N clock cycles.

29. (PREVIOUSLY PRESENTED) The method according to claim 28, further comprising the step of:

dynamically changing the values in said host register.

30. (PREVIOUSLY PRESENTED) The method according to claim 29, further comprising the step of:

searching for a specific signal pattern.

31. (PREVIOUSLY PRESENTED) The method according to claim 30, further comprising the step of:

monitoring the correctness of a bus protocol.

32. (PREVIOUSLY PRESENTED) The method according to claim 31, further comprising the step of:

implementing statistics counting to measure (i) ~~the~~ active time on bus request and (ii) ~~the~~ execution coverage ~~of the internal state machines~~.

33. (CURRENTLY AMENDED) The method according to claim 26, further comprising the steps of:

triggering and tracing based on internal signals;

triggering on ~~the~~ one or more specific values of address, data, or command bus;

dynamically changing ~~the~~ one or more host register values; and

monitoring protocol functions.